



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Su et al.

Application Serial No.: 10/689,431

Filed: October 20, 2003

For: Method for Measuring Capacitance-Voltage Curves for Transistors

Patent No.: Unassigned

Issue Date: Unassigned

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia 22313-1450

**CERTIFICATE UNDER 37 C.F.R. §3.73(b)
ESTABLISHING RIGHT OF ASSIGNEE TO TAKE ACTION**

1. The assignee of the entire right, title and interest hereby seeks to take action in the PTO in this matter.

IDENTIFICATION OF ASSIGNEE

2. The assignee of this matter is:

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY

No. 8, Li-Hsin Rd. 6

Science-Based Industrial Park

Hsin-Chu 300-77, Taiwan, R.O.C.

PERSON AUTHORIZED TO SIGN

3. Daniel R. McClure
Attorney for Assignee

4. A chain of title from the inventor(s) to the current assignee is shown below:

a. From: Hung-Der Su, Shien-Yang Wu, Yung-Shun Chen,
Kuan-Yao Wang and Sun-Jay Chang
To: Taiwan Semiconductor Manufacturing Company
Recorded in PTO: Reel: 014622 Frame: 0410

DECLARATIONS

5. I, the undersigned, have reviewed all the documents in the chain of title of the

☒ application
☐ patent

matter identified above and, to the best of my knowledge and belief, title is in the assignee identified above.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

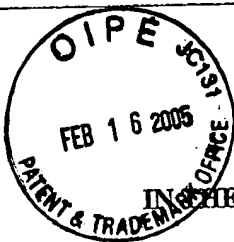
7. I, the person signing below, aver that I am empowered to sign this statement on behalf of the assignee.


Daniel R. McClure, Reg. No. 38,962

Tel. No. 770-933-9500
Customer No.: 24504

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948

Docket No. 252016-2640



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:

Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339
770-933-9500

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ASSIGNEE OF ENTIRE INTEREST

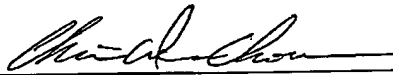
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.

8, Li-Hsin Rd. 6
Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: December 27, 2004


Chien-Wei (Chris) Chou
Director - Intellectual Property Division

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Attachment A

No.	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1	10/657,503	2002-0544	Phase Shift Assignments for Alternate PSM	9/8/03	014479/0625
2	10/425,322	2002-0382	Quartz Damage Repair Method for High-End Mask	4/29/03	014025/0791
3	10/661,746	2002-0353	Method to Shrink Cell Size in a Split Gate Flash	9/12/03	014500/0769
4	10/796,891	2002-0254B	Storage Element and SRAM Cell Structures Using Vertical FETS Controlled by Adjacent Junction Bias Through Shallow Trench Isolation	3/9/04	Recorded 014006/0344 at the parent application USP6,759,699
5	10/689,431	2002-0218	Method for Measuring Capacitance-Voltage Curves for Transistors	10/20/03	014622/0410
6	10/714,998	2002-0212	Water Soluble Negative Tone Photoresist	11/17/03	014712/0284
7	10/796,430	2002-0189	Placement and Routing Method to Reduce Joule Heating	3/9/04	015069/0548
8	10/307,646	2002-0132	Scheme for Eliminating the Channel Unexpected Turn-On During ESD Zapping	12/2/02	013547/0654
9	10/388,274	2002-0127	Light Guide for Image Sensor	3/12/03	013876/0368
10	10/256,401	2002-0064	Complementary Replacement of Material	9/27/02	013351/0995
11	10/788,175	2002-0047	Method for Making Improved Bottom Electrodes for Metal-Insulator-Metal Crown Capacitors	2/26/04	015033/0280
12	10/723,237	2001-1630	Method to Form a Robust TiCl ₄ Based CVD TiN Film	11/26/03	
13	10/755,500	2001-1596	Single Trench Repair Method with Etched Quartz for Attenuated Phase Shifting Mask	1/12/04	014896/0968
14	10/205,790	2001-1582	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	7/26/02	013148/0435

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15	10/781,182	2001-1582D	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/18/04	Recorded 013148/0435 at the parent application USP6,711,732
16	10/781,176	2001-1582B	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/18/04	Recorded 013148/0435 at the parent application USP6,711,732
17	10/782,670	2001-1582E	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/19/04	Recorded 013148/0435 at the parent application USP6,711,732
18	10/680,577	2001-1701B	SRAM Cell Design for Soft Error Rate Immunity	10/7/03	Recorded 013408/0285 at the parent application USP6,649,456
19	10/682,269	2002-0026B	Asymmetrical Reset Transistor with Double-Diffused Source for CMOS Image Sensor	10/9/03	Recorded 013422/0370 at the parent application USP6,642,076

Date: December 27, 2004



Chien-Wei (Chris) Chou
Director - Intellectual Property Division

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